IN THE CLAIMS:

Claims 3, 8-10, 22, and 26-28 were previously cancelled. Claims 1, 2, 5, 17, 19, 20 and 35 have been amended herein. All of the pending claims are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

1. (Currently amended) A multi-chip module system comprising:

a substrate having a first position having, in turn, a predetermined configuration for locating a first semiconductor device thereat and having ~~a r~~ a second position having, in turn, a predetermined configuration for locating a second semiconductor device thereat on the multi-chip module system, the second position having no semiconductor device located thereat until a semiconductor device is installed to replace a defective semiconductor device at the second position;

a first semiconductor device located in ~~the t~~ the first position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic, ~~said~~ the first semiconductor device having been burned in at ~~said~~ the first position on ~~said~~ the substrate; and

a second known-good-die located at the second position, the second semiconductor device having a second predetermined performance ~~characteristic.~~ characteristic.

2. (Currently amended) The multi-chip module system of claim 1, further comprising:

~~the a~~ a third position having the predetermined configuration for locating the second semiconductor device thereat which is substantially the same as the predetermined configuration of the first position.

3. (Cancelled)

4. (Previously presented) The multi-chip module system of claim 1, further comprising:

the second position having the predetermined configuration for locating the second semiconductor device thereat; and

the second semiconductor device having a second predetermined performance characteristic of at least substantially twice that of the first predetermined performance characteristic of the first semiconductor device.

5 (Currently amended) A multi-chip module system comprising:

a substrate having a first position having, in turn, a predetermined configuration for locating a first semiconductor device thereat, having a second position having, in turn, a predetermined configuration for locating a second semiconductor device thereat, and having a third position having, in turn, a predetermined configuration for locating a third semiconductor device thereat on the multi-chip module system, the third position having no semiconductor device located thereat until a semiconductor device is installed to replace a defective semiconductor device at another position;

the first semiconductor device located in the first position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic; and

a second known-good-die semiconductor device located in the second position of the substrate for use in the multi-chip module system, the second semiconductor device having a second predetermined performance characteristic, ~~said~~ wherein the first and second semiconductor devices have been burned in at ~~said~~ the first and second positions, respectively, on ~~said~~ the substrate.

6. (Previously presented) The multi-chip module system of claim 5, further comprising:

the third position having a predetermined configuration for locating a third semiconductor device thereat which is substantially the same as the predetermined configuration of the first position.

7. (Previously presented) The multi-chip module system of claim 5, further comprising:

the third position having a predetermined configuration for locating a third semiconductor device thereat; and

the third semiconductor device having a predetermined performance characteristic substantially similar to that of the first predetermined performance characteristic of the first semiconductor device.

8.-10. (Cancelled)

11. (Previously presented) The multi-chip module system of claim 5, wherein the first semiconductor device comprises a memory device.

12. (Previously presented) The multi-chip module system of claim 5, wherein the second semiconductor device comprises a memory device.

13. (Previously presented) The multi-chip module system of claim 5, wherein the first semiconductor device comprises a microprocessor device.

14. (Previously presented) The multi-chip module system of claim 5, wherein the second semiconductor device comprises a microprocessor device.

15. (Previously presented) The multi-chip module system of claim 5, wherein the multi-chip module system comprises a single in-line memory module system.

16. (Previously presented) The multi-chip module system of claim 5, further comprising:

a third semiconductor device; and

an adapter connected to the third semiconductor device, the adapter having a configuration for connecting the adapter to the third position on the substrate to allow connection of the third semiconductor device to the substrate.

17. (Currently amended) A multi-chip module system comprising:

a substrate having two opposing sides, ~~said~~ the substrate having a first position having, in turn, a predetermined configuration for locating a first semiconductor device thereat, having a second position having, in turn, a predetermined configuration for locating a second semiconductor device thereat, having a third position having, in turn, a predetermined configuration for locating a third semiconductor device thereat, the third position having no semiconductor device located thereat until a semiconductor device is installed to replace a defective semiconductor device at another position, and having a fourth position having, in turn, a predetermined configuration for locating a fourth semiconductor device thereat on the multi-chip module system, the fourth position having no semiconductor device located thereat until a semiconductor device is installed to replace a defective semiconductor device at another position;

the first semiconductor device located in the first position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic; and

a second known-good-die semiconductor device located in the second position of the substrate for use in the multi-chip module system, the second semiconductor device having a

second predetermined performance characteristic, ~~said~~ the first device being burned in at ~~said~~ the first position on ~~said~~ the substrate.

18. (Previously presented) The multi-chip system module of claim 17, wherein: the third position and the fourth position are on opposing sides of the substrate.

19. (Currently amended) A multi-chip module system comprising:

a substrate having a first predetermined configuration position for locating a first semiconductor device thereat and having a second predetermined configuration position for locating a second semiconductor device thereat on the multi-chip module system, the second position having no semiconductor device located thereat until a semiconductor device is installed to replace a defective semiconductor device at another position;

the first semiconductor device located in the first predetermined configuration position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic, ~~said~~ the first semiconductor device being burned in at ~~said~~ the first predetermined configuration position on ~~said~~ the substrate; and

a second known-good-die located at the second predetermined configuration position.

20. (Currently amended) The multi-chip module system of claim 19, further comprising:

~~the a~~ a third predetermined configuration position for locating the second semiconductor device thereat which is substantially the same as the predetermined configuration of the first position.

21. (Previously presented) The multi-chip module system of claim 19, further comprising:

the third predetermined configuration position having a predetermined configuration for locating the second semiconductor device thereat; and

the second semiconductor device having a predetermined performance characteristic substantially similar to that of the first predetermined performance characteristic of the first semiconductor device.

22. (Cancelled)

23. (Previously presented) A multi-chip module system comprising:

a substrate having a first predetermined configuration position for locating a first semiconductor device thereat, having a second predetermined configuration position for locating a second semiconductor device thereat, and having a third predetermined configuration position for locating a third semiconductor device thereat on the multi-chip module system, the third position having no semiconductor device located thereat until a semiconductor device is installed to replace a defective semiconductor device at another position;

the first semiconductor device located in the first predetermined configuration position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic; and

a known-good-die second semiconductor device located in the second predetermined configuration position of the substrate for use in the multi-chip module system, the second semiconductor device having a second predetermined performance characteristic.

24. (Previously presented) The multi-chip module system of claim 23, further comprising:

the third predetermined configuration position for locating the third semiconductor device thereat which is substantially the same as the predetermined configuration of the first position.

25. (Previously presented) The multi-chip module system of claim 23, further comprising:

the third predetermined configuration position for locating the third semiconductor device thereat; and

the third semiconductor device having a third predetermined performance characteristic substantially similar to that of the first predetermined performance characteristic of the first semiconductor device.

26.-28. (Cancelled)

29. (Original) The multi-chip module system of claim 23, wherein the first semiconductor device comprises a memory device.

30. (Original) The multi-chip module system of claim 23, wherein the second semiconductor device comprises a memory device.

31. (Original) The multi-chip module system of claim 23, wherein the first semiconductor device comprises a microprocessor device.

32. (Original) The multi-chip module system of claim 23, wherein the second semiconductor device comprises a microprocessor device.

33. (Original) The multi-chip module system of claim 23, wherein the multi-chip module system comprises a single in-line memory module system.

34. (Previously presented) The multi-chip module system of claim 23, further comprising:

an adapter connected to the third semiconductor device, the adapter having a configuration for connecting the adapter to the third predetermined configuration position on the substrate to allow connection of the third semiconductor device to the substrate.

35. (Currently amended) A multi-chip module system comprising:

a substrate having two opposing sides, ~~said~~ the substrate having a first predetermined configuration position for locating a first semiconductor device thereat, having a second predetermined configuration position for locating a second semiconductor device thereat, having a third predetermined configuration position for locating a third semiconductor device thereat, the third predetermined configuration position having no semiconductor device located thereat until a semiconductor device is installed to replace a defective semiconductor device at another position, and having a fourth predetermined configuration for locating a fourth semiconductor device thereat on the multi-chip module system, the fourth predetermined configuration position having no semiconductor device located thereat until a semiconductor device is installed to replace a defective semiconductor device at another position;

the first semiconductor device located in the first predetermined configuration position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic; and

a known-good-die second semiconductor device located in the second predetermined configuration position of the substrate for use in the multi-chip module system, the second semiconductor device having a second predetermined performance characteristic.

36. (Previously presented) The multi-chip system module of claim 35, wherein: the third predetermined configuration position and the fourth predetermined configuration position are located on opposing sides of the substrate.